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Designing, Simulating, and Layout of an RFIC Mixer in a 130 nm SiGe Process

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Designing, Simulating, and Layout of an RFIC Mixer in a 130 nm SiGe Process

Undergraduate Honors Thesis

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Abstract:

Wireless devices are becoming increasingly popular each day ranging from smartphones to Amazon Echo's to wireless sensors in industry. While all of these devices are quite different in their functions and purposes, they all rely on wireless communication heavily and signal modulation techniques. One component typically seen in wireless applications like this are mixers, which are used to modulate the signal being sent and received. This thesis details the design, simulation, and layout of a radio frequency integrated circuit mixer in a 130 nanometer silicon germanium process. While the fabricated mixer did not perform to standards, many things were learned along the way about RFIC design and how future redesigns could be improved to result in better performance.

Acknowledgement:

I would like to first thank my mother and grandmother for supporting me throughout my academic career along with everything else in life. Second, I would like to thank Dr. Mantooth for giving me the opportunity to work with his integrated circuit design group for the past year. Next, I would like to thank Affan Abbasi and Marvin Suggs for guiding me throughout this project and integrating me into the RF corn project team. Finally, I would like to thank Lauren Weatherly for supporting me in everything I do and helping motivate me to do my best and go out of my comfort zone.

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Introduction:

This thesis is intended to go over the design, simulation, and layout of a radio frequency integrated circuit (RFIC) mixer in a 130 nm silicon germanium process. The goal of this project was to become familiar with the process of designing, simulating and laying out an RF device. While the mixer was not going to be used in the final system of the project, going through the process once allows for the user to learn about some of the common pitfalls of RFIC designs along with learning about some of the different simulations related to RF designs that are not typically used in DC or lower frequency designs.

To begin, a brief intro to mixer theory will be given detailing how a mixer works and why they are important. Following that, more detail will be given about the specific topology being used for this design. Next, the simulations used to characterize a mixer will be discussed. The process for laying out the mixer and how it could have been improved will follow that. Finally, the results of the mixer designed along with how it could further be improved will be explained.

Mixer Theory:

Mixers are a type of RF device that is used to modulate two input signals together to output one signal of a different frequency. This output frequency, also known as the intermediate frequency (IF) signal, is composed of two main frequency elements based on the input radio frequency (RF) signal and the local oscillator (LO) signal. The first frequency component is equal to the summation of the RF and LO frequency's while the second

component is based off the difference between the two frequencies. Typically, we only want one of these signals and the one we want determines what type of mixing modulation we are performing. When we are taking the difference between RF and LO and outputting a frequency that is lower than both of our input signals, we are performing a down conversion. However, when we take a low RF frequency and mix it with the LO signal, we will see a signal with the summation of the RF and LO frequency and another that is the difference between the two input frequencies. This type of mixing is referred to as up converting. Fig. 1 below illustrates both of these types of mixing. [1]

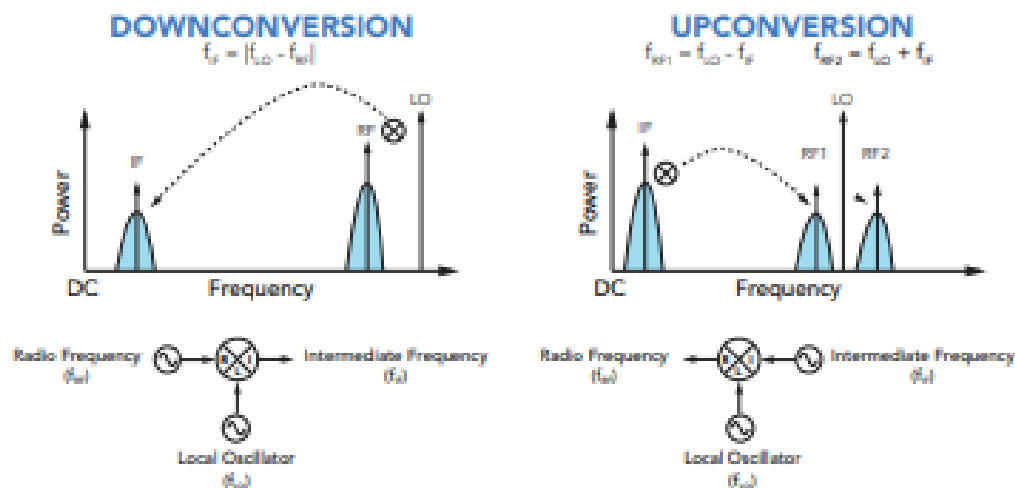


Fig. 1: An illustration of both down converting and up converting mixing.

After we have mixed our signals, we will typically filter out the unwanted frequency's in our signal. This is because our output signal will be composed of both our desired frequency along with other elements such as noise along with multiple orders of harmonics of our signal. We can filter out these unwanted elements by applying either a band pass, low pass, or high pass filter to our output.

Knowing why we modulate two signals in this way is also very important to understand.

We use mixers to modulate a desired signal to either higher or lower frequencies which each have their own benefits. Modulating to a higher frequency allows for the following RF components such as antenna's to be smaller which is a very critical factor in current designs today. Also, the bandwidth is directly proportional to the frequency which means if we need to transmit more data then we would need to step our frequency up. [2] However, the big disadvantage of transmitting at higher frequencies is that higher frequencies have higher losses when propagating through larger objects such as buildings and walls. This results in us either having to accept having less range or having to increase the level power we transmit so that we could obtain the same range as we can get with lower frequencies. In RF systems, when a mixer is used, there will be a mixer in both the transmitter and receiver systems. This normally involves the transmitter mixer performing an up conversion of the data to a higher frequency so that the following RF circuitry can remain small and so that we can achieve a higher bandwidth. In the receiver set up we then have a similar mixer performing a down conversion to demodulate the signal we received. To perform this successfully, the LO signal for both the transmitter and receiver must be the same. This ensures that we receive the data at the same frequency as when we had transmitted it. An example of a transmitting and receiving system using a mixer is shown below in Fig. 2. [3]

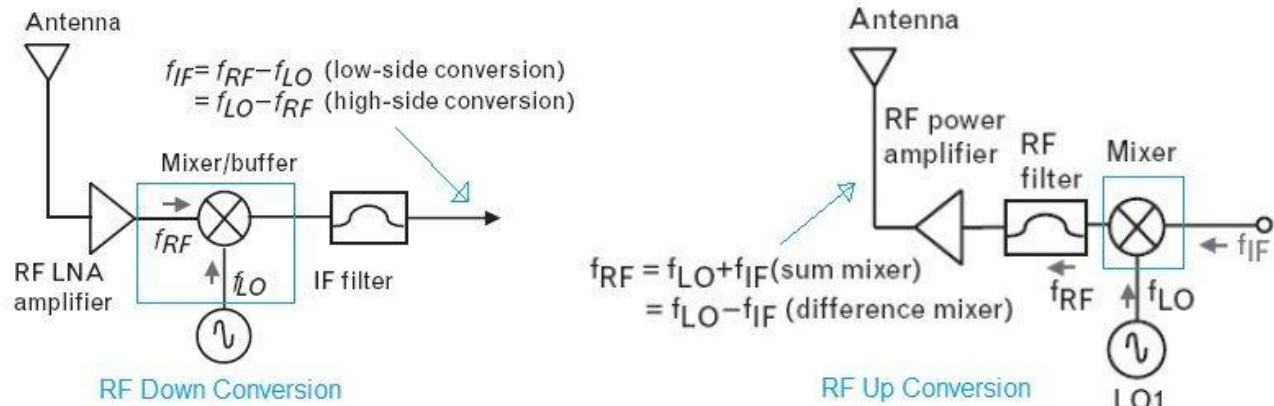


Fig. 2. A basic system diagram of a receiver (left) and transmitter (right) using an RF mixer.

Design:

RF mixers come in many different topologies ranging from passive or active and single or doubled ended balanced. While the mixer designed in this thesis is a double ended balanced active mixer, also known as a Gilbert mixer, the other mixer topologies will be briefly discussed. When calculating values for your components you will need to know the frequencies of your different signals. Our RF signal was 425 MHz, our LO was 400 MHz, and since we are wanting to perform a down conversion, our IF signal will be 25 MHz.

To start, passive mixers are composed only of passive components which are resistors, capacitors, inductors, and diodes. The common passive mixer topology is composed of 4 diodes in a diamond configuration and two center tapped transformers. [4] However, the transformers can be removed if either the RF or the LO signal is differential since the transformers here are being used to convert single ended inputs into differential inputs. If this is not integrated into the chip, then this can be performed externally through a balun. The large downside to using a passive mixer is that the gain will never be greater than 0 dB along with there being poor port-

to-port isolation. The passive topology described is shown in Fig. 3. Active mixers on the other hand though have better gain and port-to-port isolation.

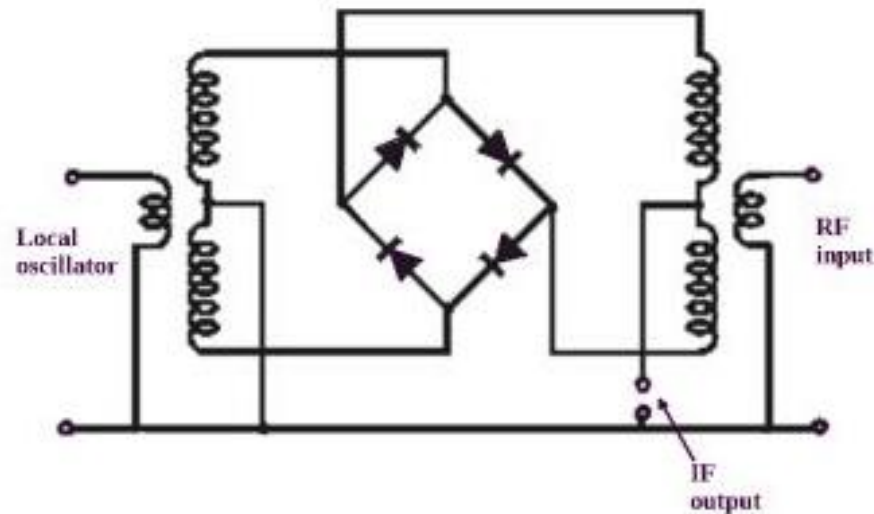


Fig. 3: A double balanced passive mixer topology.

Another form of classification of mixer topologies is whether they are single ended balanced or double ended balanced. Both types offer their own benefits, but a double ended mixer was chosen for this design. The difference between a single and double ended balanced mixer is based on how many differential stages there are in the system. A single ended mixer will have a differential LO input while the double ended has differential inputs on both LO and RF. While the single ended topology has better noise isolation, the double ended topology has better linearity along with the added benefit of having all even order harmonics being naturally removed which is why this type of topology was chosen. The basic topology of a double balanced active mixer is commonly referred to as a Gilbert cell mixer which is the one being designed along with being shown in Fig. 4. [5]

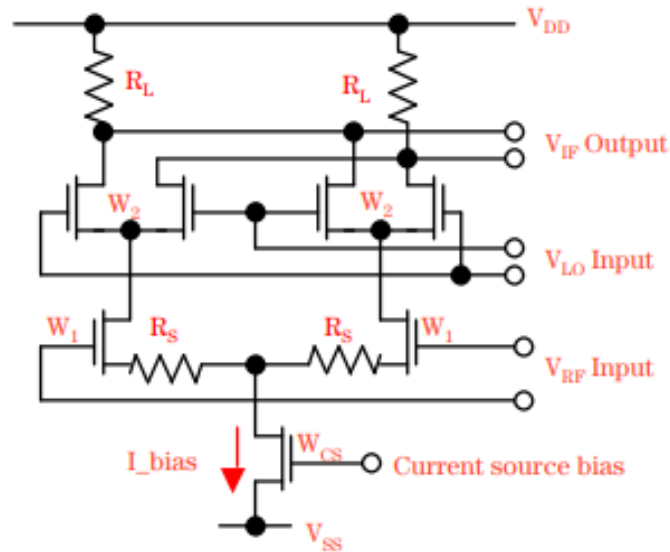


Fig. 4: A double balanced active mixer, also known as a Gilbert cell mixer.

The Gilbert cell can be broken down into three main stages. The first stage is the current biasing stage at the bottom circuit which sets the current for the mixer. Above that there is the gain stage which is where the differential RF signal is brought in. These transistors account for most of the gain of the system which means they should be sized accordingly. The gates of these transistors are driven by our differential RF signal. The third stage above the gain stage is our switching stage. Here, a differential pair of transistors is connected to each side of the gain stage and is being driven by a differential LO signal. Since we have two sets of differential pairs, we take our IF signal differentially between the two drains of the transistors that are being driven by the positive end of the LO signal.

While the previously proposed Gilbert cell mixer design is good, it can be further modified to change its parameters to better fit different applications. The main trade offs between the different parameters of RFIC designs can be illustrated in the RF design hexagon seen in Fig. 5. [6] When choosing what type of mixer topology you want to implement, it is

important to know what your critical parameters are and which ones are not. The critical parameters will be what dictates which type of topology you use. There are many different modifications that you can make to a Gilbert cell mixer to alter its parameters but that will not be discussed in detail in this thesis. The effects on different mixer parameters based on their topologies is illustrated in Table I which was pulled from a study by Rahul Sharma, Abhay Chaturvedi, and Manish Kumar. [6] While these other modifications are beneficial to know, the mixer designed and tested in this thesis was using a basic Gilbert cell topology which was shown in Fig. 4.

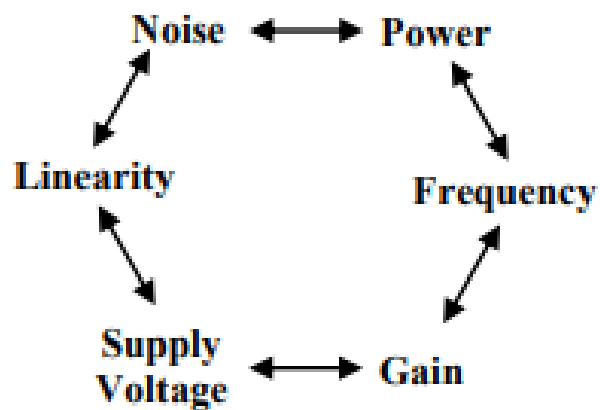


Fig. 5: The RFIC parameter tradeoff hexagon.

Table I: Comparison of Different Types of Mixer Techniques

Techniques	Multi-Tanh	Current Bleeding	Folded Cascode	Bulk-Driven	CCPD	MGTR	Switched Biasing
Linearity	High	High	Moderate	Low	High	Moderate	Low
Noise Figure	Moderate	High	High	High	Moderate	Moderate	Low
Conversion Gain	Low	Moderate	Moderate	Moderate	Moderate	Low	Moderate
Power Consumption	High	High	Low	Low	High	High	High

For the sizing of our components that we used for our design we followed the mixer tutorial by Steve Long. [5] To assist in the design process, MATLAB was used to quickly assess equations to find the optimum values. This was mainly implemented for optimizing the values for the inductor and the resistor that made up the Z_s component in between the gain stage and the current biasing transistor so that the RF input impedance was 50Ω . Using the equations in Steve Long's tutorial, we swept both the values of the resistor and the inductor and found which combinations gave us an RF input impedance of 50Ω . Once these sets of values were found, we selected the best set based off their effect on the linearity of the system and how much area they would take up in the layout. The final values that were selected for the different components can be found in Table II.

Table II: Final Component and Power Supply Values

Component/Supply Name	Value
R_L	382.11 Ω
Transistor Lengths (L)	240 nm
Transistor Total Width (W)	1.78 mm
R_S	15.04 Ω
L_S	10.1 nH
V_{DD}	2 V
$P_{Consumed}$	6.52 mW

Simulation:

While there are many different topologies to choose from, the process for simulating each of the different topologies will be the same. Understanding the types of simulations you run to characterize a mixer is important because they are not the same type of simulations that you would typically use to analyze a digital or a low frequency analog circuit. Some of the important parameters that are related to mixers are its conversion gain, the noise figure, its output frequency spectrum, the port to port isolation, and the S11 parameter. The exact process for performing all of these simulations will not be discussed in this thesis though since the process will be different depending on which software you are using. However, what each parameter represents and what we expect to see will be discussed along with comparing these expectations to results of the mixer designed.

One of the first types of simulations that you run is the conversion gain/loss. This value is typically represented in dB or dBm depending on your power levels and the desired value is dependent on your application and the type of mixer. The conversion gain/loss is simply the ratio of the IF power to the RF power and then converted to dB/dBm. This means that a conversion gain is when we see higher IF levels than what we had inputted in the RF side (Positive dB/dBm values) while a conversion loss is when IF is lower than RF (negative dB/dBm values). While a high conversion is good in some cases, high gain means higher power consumption along with the potential risk of saturating your devices following the mixer. Therefore, the ideal conversion gain would only be a few dB but can be higher if need be for the application. When simulating conversion gain, it is also important to note that the conversion gain can be affected by many different factors. For example, we simulated the conversion gain for when we swept the LO power (Fig. 6) and the RF frequency (Fig. 7). For the conversion gain vs LO power, we are aiming to see at which LO input power do we get the best gain at. For this specific design we can see that the max conversion gain was obtained when LO was 9.4 dB and we achieved a conversion gain of about -43 dB. Here we can see that the conversion gain is extremely low which be addressed later. Using that value for LO we just obtained we can now go ahead and set the value for the LO input power so that we achieve the highest possible conversion gain. For the simulation where we swept the RF frequency, the main thing we are able to gain from this is that as we increase our frequency there is a decline in the conversion gain of the system. This is important to know for when you begin testing your mixer over frequencies other than your target frequency.

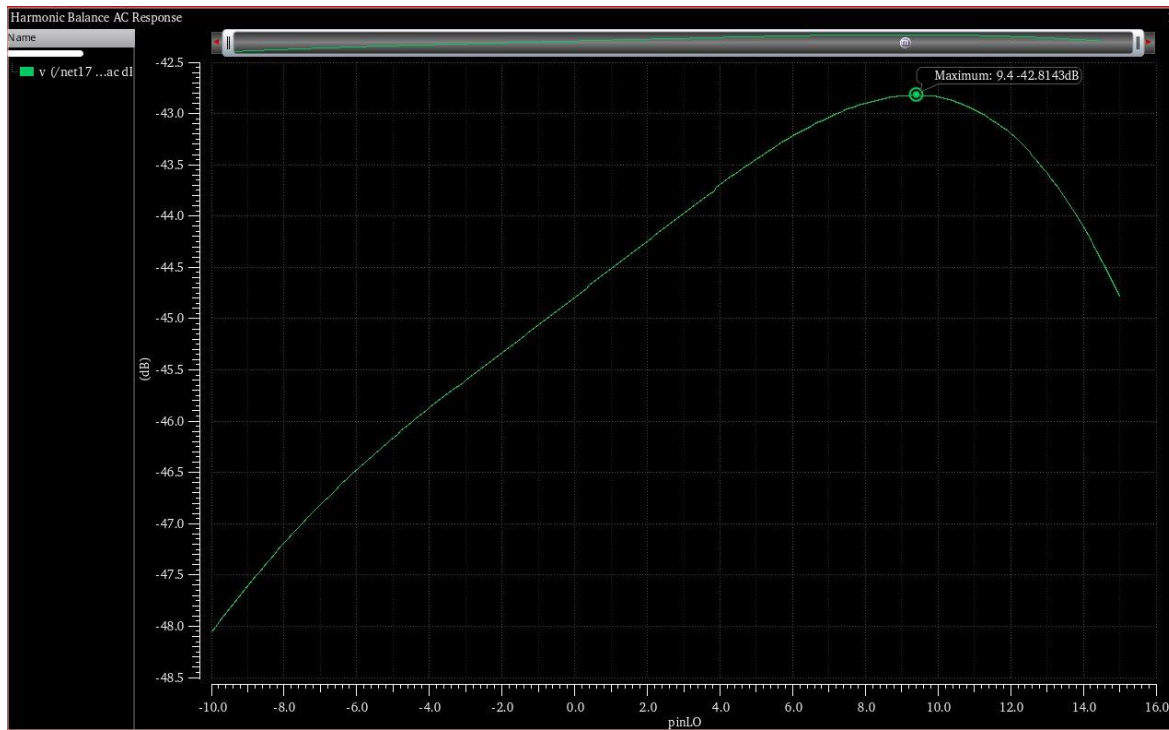


Fig. 6: Conversion gain vs. LO input power.

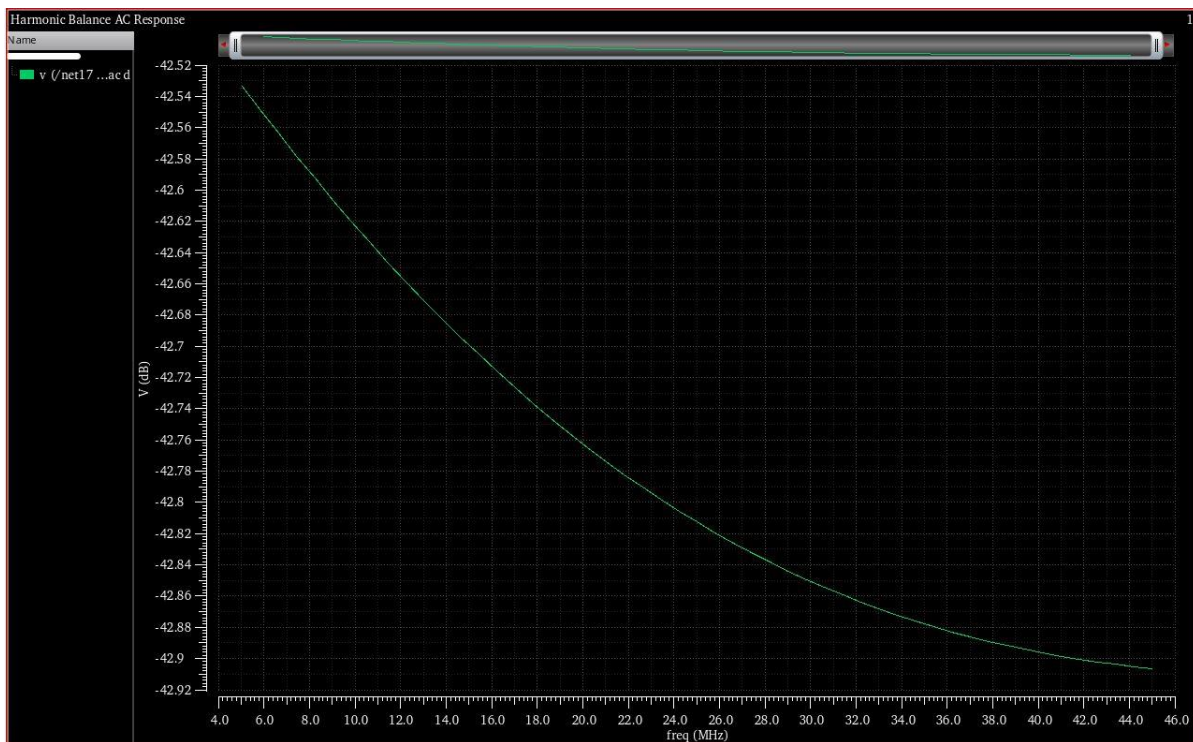


Fig. 7: Conversion gain vs. RF input frequency.

The next simulation is directly related with the conversion gain and that is the noise figure. The noise figure is a representation of how well the system handles noise. Since noise is obviously an unwanted element, we are aiming to see very little noise at the output of our system. While we do want the level of noise on the output to be as small as possible, we sometimes must decide as to how much is acceptable. This comes in to play when we must decide how large we want our conversion gain because the level of our output noise is directly related to the conversion gain of our system. If we are in need of a very large conversion gain, then we will not have as good of a noise figure than if we were to use a similar device with a lower gain. For the mixer designed, we can see the results of our output noise in Fig. 8. These results show that the noise voltage level is very low across the simulated frequencies however when we compare this value to our actual IF signal based off the conversion gain, we can see that the noise is very high.

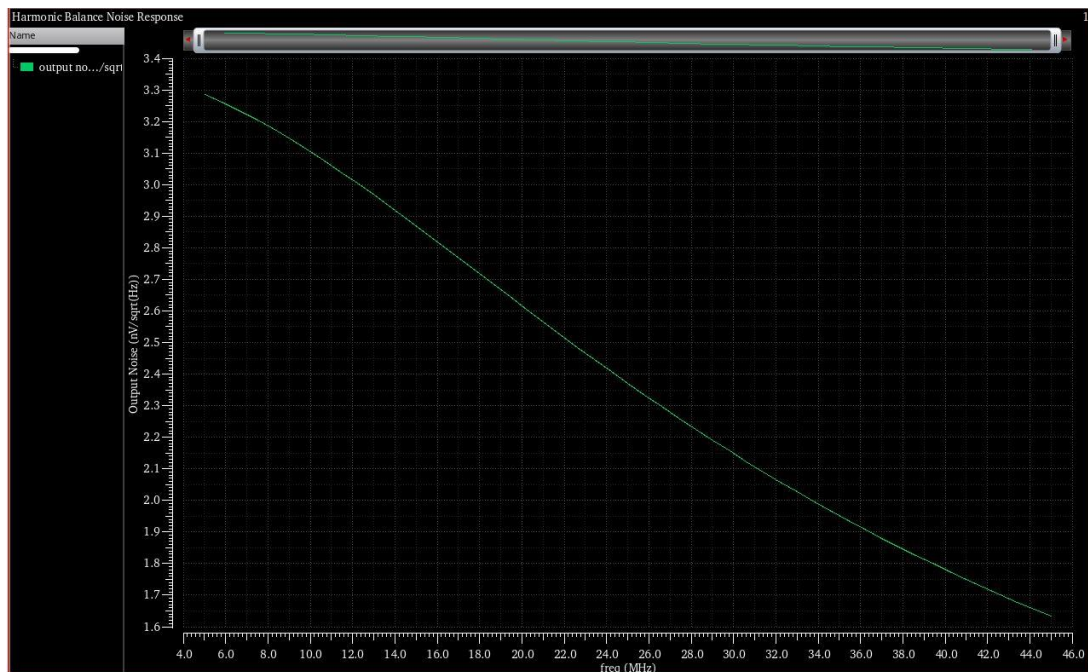


Fig. 8: IF noise vs. IF frequency.

Another parameter that is important to simulate is the output frequency spectrum. This type of simulation is used to see the different frequency elements in your signals. Here, you will typically want to see very high values for your intended signal and then very low values for the unwanted frequencies. This simulation is important to run because you are not able to see every frequency in your signal in a traditional transient simulation because all the frequencies are mixed together into one signal. Looking at this simulation you can observe how strong the side frequencies are and whether a filter will be needed to isolate the desired signal from the unwanted frequencies. The frequency spectrum results for the designed mixer are shown in Fig. 9 with the IF frequencies being represented in pink and the RF frequencies being represented in green. Looking at these results we can see that there is very little side frequencies for our RF signal and almost no side frequencies in our IF signal which is very good and what we are wanting.

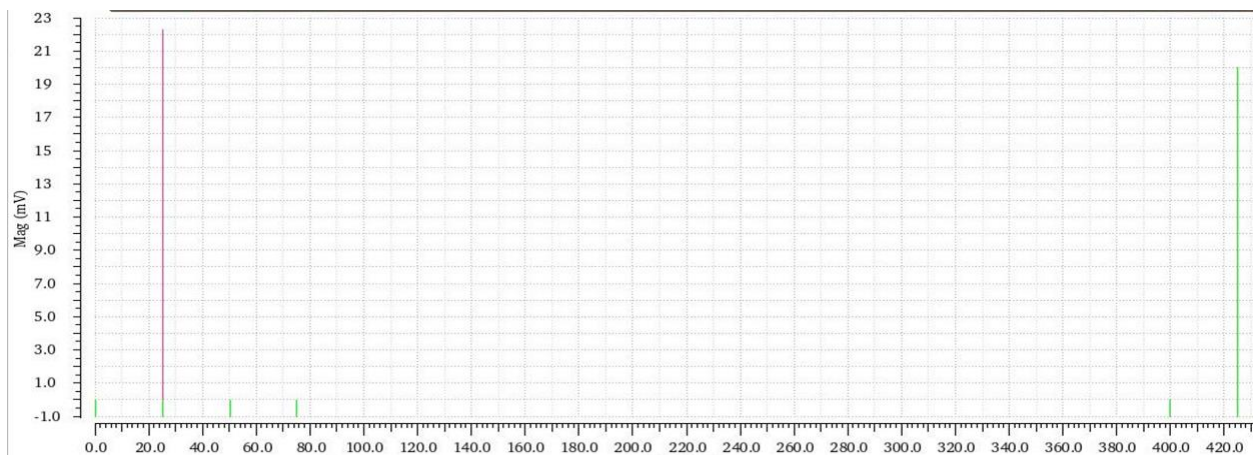


Fig. 9: Frequency spectrum for IF (pink) and RF (green).

The next factors to test for the port-to-port isolation between each of the three ports. There are three main types of isolation we check for and that is LO-IF, LO-RF, and RF-IF. These values are measured in dB and we want these to be as low as possible. The effects of having poor isolation is different for each port pair but none are beneficial to the system which is why we want there to be good isolation. With poor LO-IF isolation we see the LO signal contaminate the IF signal which lowers the quality of our output signal. Poor LO-RF isolation can cause issues because the LO signal will begin to contaminate the RF signal line which will feed into the other devices connected to the mixer. [7] The following figures show the LO-IF (Fig. 10), the LO-RF (Fig. 11), and RF-IF (Fig. 12) isolation for the mixer. Looking at these results, we can see that we have poor DC isolation between the LO-IF and the LO-RF ports which results in us having a DC offset. However, the isolation for all other frequencies for all ports is very good.



Fig. 10: LO-IF isolation results.

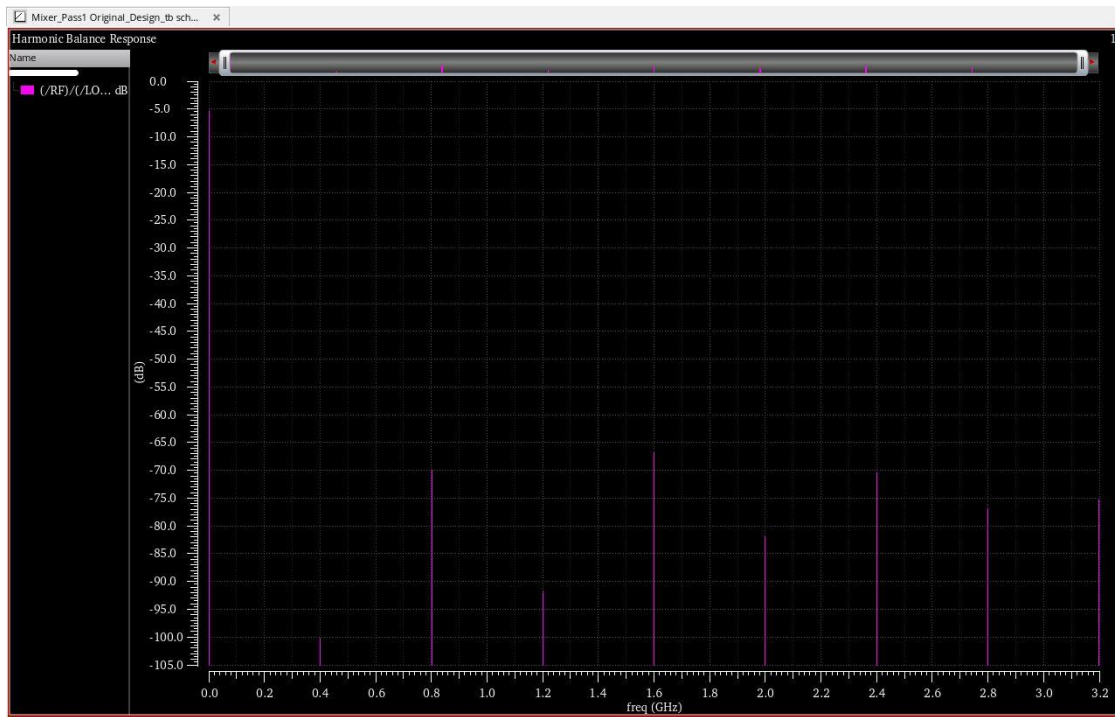


Fig. 11: LO-RF isolation results.

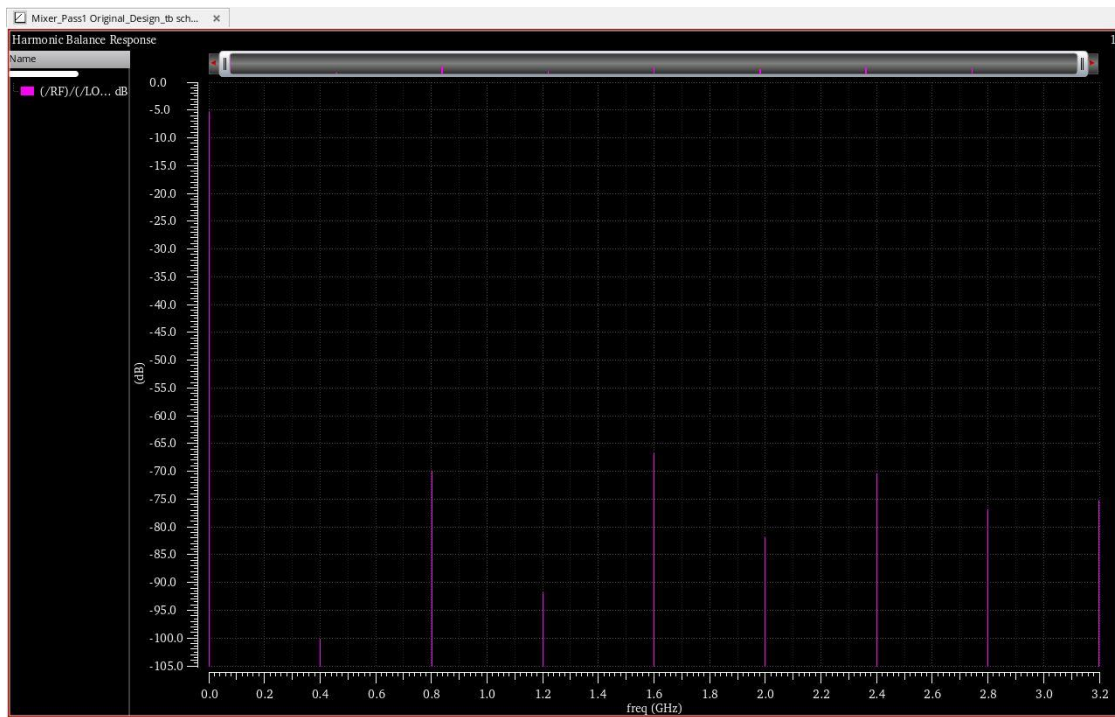


Fig. 12: RF-IF isolation results.

Finally, the last important parameter to test for is the S11 value for our RF input. While there are other S-parameters we can simulate for, the most important one is our S11. The S11 parameter is one of the most important values to test for in any RF circuit because this value relates to the devices VSWR and reflection coefficient which determines how much power is reflected back when we connect another device to it. A common value to aim for with a S11 value is $50\ \Omega$ since it is common in industry however this can be adjusted to another value if desired. This is a simple simulation to run however its value holds a lot of meaning therefore it is extremely important that this simulation is ran. In this design, we selected internal values for the Z_s component so that our RF input would already be matched to $50\ \Omega$. After running the simulation and plotting it on a Smith chart we find that our input impedance is around $49\ \Omega$ which is acceptable for our design.

Layout:

Once the simulation values are at an acceptable value for your application, the final stage is to layout the design. While this may not seem like an important factor to the final results, an intelligent and strategic layout is critical for a successful fabrication of the final device. While some of the strategies used to create the layout seen in Fig. 13 were good, there were other techniques that could have been implemented to further improve the design. A technique common to a lot of IC design is placing the traces and the metal routes at the minimum spacing to save space. This was not implemented in the current layout which means we would have been able to save a lot of space by placing the transistors closer together and spacing the routing lines closer. Something not relevant in all RF designs but is with this design

is placing your inductors orthogonally to each so as to prevent them from coupling together. Coupled inductors will cause the inductance value to change which means that our input would no longer be matched to $50\ \Omega$. Another technique is routing longer traces on the metal layer with the lowest resistance which in this process was the top layer (orange in the layout). Putting these longer traces on the layer with the least resistance minimizes the resistance along with other parasitic elements. These parasitic elements have a very negative on RF circuits so finding ways to minimize it are imperative to a successful design. Finally, another technique would be to minimize the amount of crossing traces and when they do cross have them spaced as far apart as possible. This is another technique for minimizing the parasitic capacitance. Once the layout passes the design rule check (DRC) and the layout vs schematic (LVS) then it is important to run a RLC parasitic extraction of the layout. The extraction will factor in all of the parasitic elements of the system and recreate the layout with those factored in. This new extraction can then be used in the previous simulations to see how the mixer performs with the parasitic factors included.

If I were to redo the layout, I would first begin by focusing on trying to place the transistors as close as I could to each while leaving enough space for routing. This would already start to save space. However, for the traces I would allow for the traces to be a longer if it meant that it would prevent a lot of crossing. The reduced capacitance from not crossing is worth the small amount of added resistance to the trace. Finally, I would make the V_{DD} and the GND traces a lot wider to reduce the parasitic resistance and inductance of the trace.

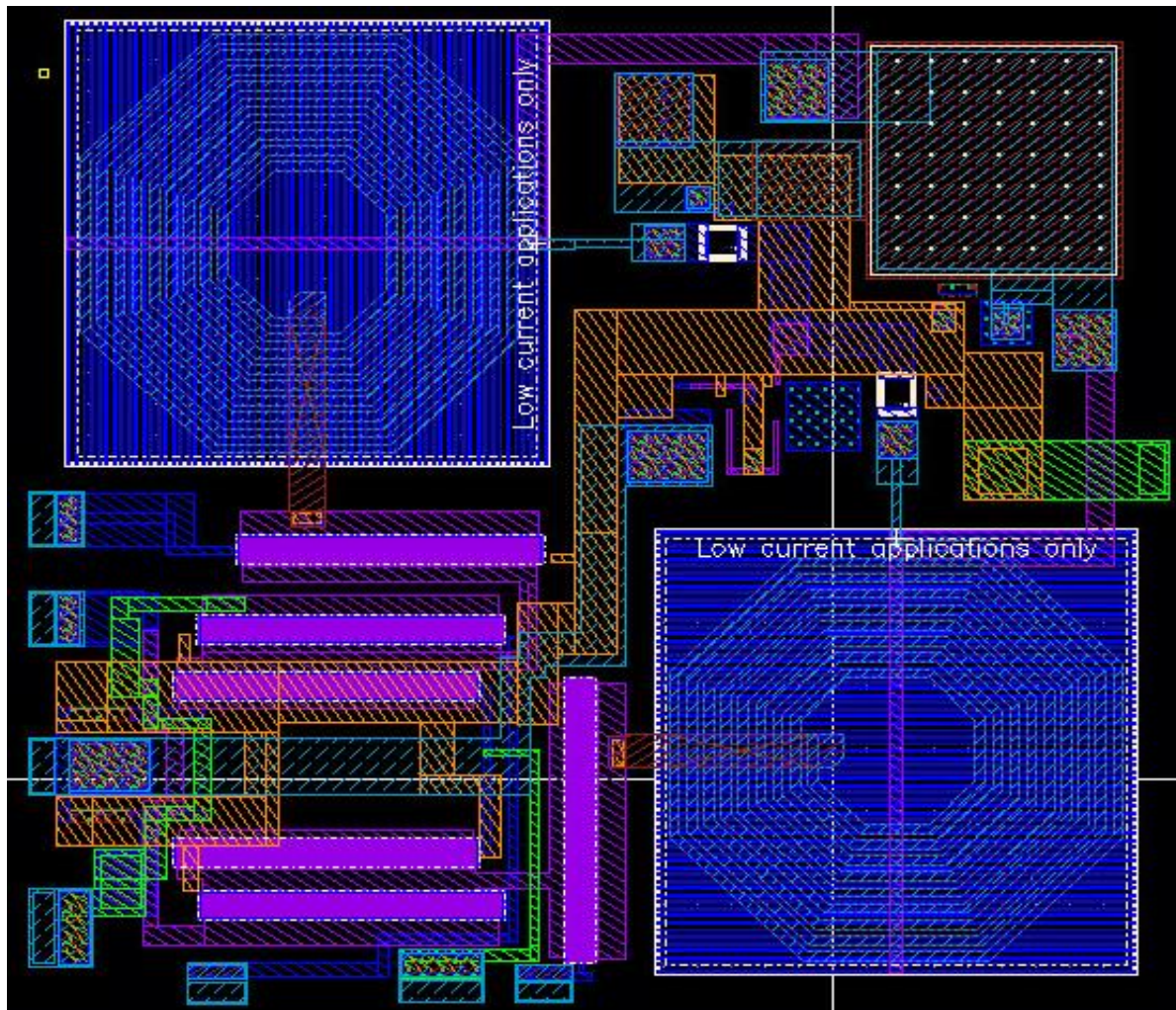


Fig. 13: Final layout of the mixer.

Results:

Looking at the results of the simulations, we can see that the mixer does not perform to an acceptable level. This is found mainly in the conversion gain section where we have a gain in the -40 dB range. However, the port-to-port isolation is very good so during a redesign the goal would be to increase the conversion gain of the system to an acceptable level without reducing the port-to-port isolation. In regards to the layout, spacing the transistors closer together and

being more strategic with the routing could result in a smaller layout with less parasitic elements.

For increasing the conversion gain, we have found that decreasing the width of the switching stage transistors can improve the gain dramatically. When following the tutorial by Steve Long it states that the width for the transistors in both the gain and switching stage should be the same. However, this results in a very poor gain as seen in the previous simulations. After decreasing the switching stage widths, we then get a conversion gain of about -20 dB. While that is still not an acceptable gain, it is a step in the right direction towards improving the design.

Conclusion:

While we did not end with a successful mixer, we did however learn a lot about how a mixer operates, how to perform different simulations, and some things to consider when laying out an RF design. This is useful to understand when doing either a mixer redesign or any other kind of RFIC design. For this mixer, the best method for improving the gain would be to start back over at the designing stage and find new ways to improve the gain.

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